PATENT
790001-2034

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Noriaki MATSUNAGA et al.
U.S. Serial No.	:	Not Yet Assigned
Filing Date	:	July 28, 2003
For	:	***SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD***
Group Art Unit	:	Not Yet Assigned

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New York, New York 10151

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Date of Deposit: July 28, 2003

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INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application
Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

The Examiner's attention is respectfully invited to review the following enclosed and listed document which is also listed on the accompanying Form PTO-1449, enclosed in duplicate.

OTHER REFERENCES

1. K. Higashi, et al., "*A Manufacturable Copper/Low-k SiOC/SiCN Process Technology for 90nm-node High Performance eDRAM*," PROCEEDINGS OF THE 2002 INTERNATIONAL INTERCONNECT TECHNOLOGY CONFERENCE, June 2002, pp. 15-17.

REMARKS

Pursuant to Rule 37 C.F.R. §1.97(b)(3), an Information Disclosure Statement shall be considered by the Patent Office filed before the mailing date of a first Office Action on the merits.

This Information Disclosure Statement is not a representation that the document cited herein is considered most pertinent, or that a search has been undertaken, or that the cited document is indeed prior art. The Examiner is invited to undertake an independent search. Applicants assert that the claimed invention is patentable over this document.

Applicants respectfully request that the Examiner consider and make of record the document cited herein and that a copy of Form PTO-1449, appropriately initialed by the Examiner, be returned to Applicants' attorney.

It is believed no fee is due, however, the Examiner is authorized to charge any deficit or credit any overpayment to Deposit Account No. 50-0320.

Respectfully submitted,

FROMMER LAWRENCE & HAUG LLP
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Based on Form PTO-1449
(3/90)

LIST OF REFERENCES CITED BY APPLICANT

(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
790001-2034	Not Yet Assigned
APPLICANTS	
Noriaki MATSUNAGA et al.	
FILING DATE	GROUP
July 28, 2003	Not Yet Assigned

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
							YES	NO

OTHER PRIOR ART (Including Author, Title, Date, Pertinent Pages, Etc.)

			K. Higashi, et al., "*A Manufacturable Copper/Low-k SiOC/SiCN Process Technology for 90nm-node High Performance eDRAM*," PROCEEDINGS OF THE IEEE 2002 INTERNATIONAL INTERCONNECT TECHNOLOGY CONFERENCE, June 2002, pp. 15-17.

			EXAMINER

	DATE CONSIDERED

* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.